Claims

We claim:

1. An analog-to-digital converter (ADC) offset calibration system in a digital capacitive isolation system having a powered circuit on a first side of a capacitive isolation barrier and an isolated circuit on a second side of the barrier, wherein digital signals are transmitted across the isolation barrier, and wherein an ADC requiring calibration is located on the second side of the isolation barrier, the ADC offset calibration system comprising:

a digital integrator connected to receive an output signal from the ADC and to provide an integrated offset calibration signal;

a data register connected to receive and hold the integrated offset calibration signal, the data register outputting a held offset calibration signal;

a digital-to-analog converter (DAC) having an input connected to receive the held offset calibration signal and having an output providing an analog offset calibration signal; and

a hybrid circuit including a signal path connecting the output of the DAC to an input of the ADC;

whereby the analog offset calibration signal is connected to the input of the ADC requiring calibration.

2. The calibration system of claim 1, wherein the ADC being calibrated is a delta-sigma ADC.

3. The calibration system of claim A, further comprising a fixed ADC bias source connected to an input of the ADC to provide a fixed ADC bias level to a signal passing through the ADC.

4. The calibration system of claim 3, further comprising a negative fixed ADC bias source connected to an output of the ADC for removing the fixed ADC bias level from the signal passing through the ADC.

5. The calibration system of claim 1, wherein the digital to analog converter comprises a delta sigma modulator coupled to a one-bit digital to analog converter.

6. The calibration system of claim 5, wherein the delta sigma modulator is located on the first side of the isolation barrier and the one-bit digital to analog converter is located on the second side of the isolation barrier.

7. The calibration system of claim 1, wherein the ADC is located on the second side of the isolation barrier and the integrator is located on the first side of the isolation barrier.

8. The calibration system of claim 1, further comprising a fixed DAC bias source connected to combine a fixed DAC bias signal with the output of the digital integrator, and wherein the data register is connected to receive and hold the combination of the integrated offset calibration signal and the fixed DAC bias signal.

9. The system of claim 8, further comprising a negative fixed DAC bias source connected to an output of the digital to analog converter for removing the fixed DAC bias signal from an output signal from the digital to analog converter.

10. The system of claim 1, wherein the hybrid circuit comprises a calibration mode switch adapted to disconnect the hybrid circuit from an incoming data signal while ADC offset calibration is performed.

11. A method of performing analog-to-digital converter (ADC) offset calibration in a digital capacitive isolation system, comprising:

maintaining a data input signal into the ADC being calibrated at a level of zero;

integrating an output signal from the ADC to provide an integrated offset calibration signal;

holding the integrated offset calibration signal in a data register;

converting the integrated offset calibration signal from a digital signal to an analog offset calibration signal using a digital-to-analog converter (DAC);

adding the analog offset calibration signal to said data input signal, using a hybrid circuit signal path to connect the analog offset calibration signal from the DAC to an input of the ADC; and

latching the integrated offset calibration signal in the data register when the output signal from the ADC becomes zero.

12. The method of claim 11, further comprising adding a fixed ADC bias signal to said data input signal before it enters the ADC, and removing the fixed ADC bias signal from the ADC output signal.

13. The method of claim 11, further comprising adding a fixed DAC bias signal to said integrated offset calibration signal, and storing the combined signal in the data register; and removing the fixed DAC bias signal from a DAC output signal in order to generate the analog offset calibration signal.

14. The method of claim 11, further comprising forcing an input data signal to the DAC to zero during performance of the calibration method.

15. The method of claim 11, wherein the analog offset calibration signal is attenuated by the hybrid circuit signal path.

16. A telecommunication hybrid circuit for processing an analog transmitted signal to be coupled to a communication system at a transmitter node and an analog received signal received from the communication system at a receiver node, wherein the received signal includes a portion of the transmitted signal, the hybrid circuit comprising:

a transmitter amplifier having an output coupled to the transmitter node;

a receiver amplifier having an input coupled to the receiver node;

an attenuated signal path between the input of the transmitter amplifier and a subtractive input of the receiver amplifier; and

a calibration mode switch coupled between the receiver amplifier and the receiver node, the calibration mode switch alternately connecting the input of the receiver amplifier to the receiver node or to a preselected signal.

17. The hybrid circuit of claim 16, wherein the preselected signal is a ground signal.

18. The hybrid circuit of claim16, wherein the transmitter node and the receiver node are output pins of an integrated circuit that comprises the transmitter amplifier and the receiver amplifier.

19. The hybrid circuit of claim 16, wherein the attenuated signal path comprises a resistor connected between the input of the transmitter amplifier and a subtractive input of the receiver amplifier.

20. The hybrid circuit of claim 16, wherein the input of the transmitter amplifier is connected to an output of a digital-to-analog converter, and the output of the receiver amplifier is connected to an input of an analog-to-digital converter.